12th International School on the Effects of Radiation on Embedded Systems for Space Applications, (SERESSA'2016), Montreal, Canada
November 7 – November 10
Final Program

	Monday	Tuesday	Wednesday	Thursday
8:00 – 9:00	Registration	Registration **(session starts at 8:30)**	Registration **(session starts at 8:30)**	Registration
9:00 – 10:30	**Opening Remarks** P. Fouillat (IMS, France) & R. Velazco (TIMA, France) **Opening Local Chair** C. Thibeault (ETS, Canada) **Technical Program Overview** O. Ait Mohamed (Concordia Univ., Canada) **Single Event Effects (SEE): Mechanisms and Classifications** S. Buchner (NRL, USA)	**Space Activities, Current Projects and Strategic View in Canada** E. Gloutnay (CSA, Canada) **Nanosatellites Future in France** M. Barthelemy (CSUG, France) **System Hardening and Real Applications** M. Pignol (CNES, France)	**Radiation Effects Hardness Assurance** S. Buchner (NRL, USA) **COTS in Space: Constraints, Limitations and Disruptive Capability** M. Pignol (CNES, France)	**New Developments in FPGA: SEUs and Fail-Safe Strategies From the NASA Goddard Perspective** M. Berg (NASA, USA)
10:30-11:00	Break & Poster Session	Break & Poster Session	Break & Poster Session	Break & Poster Session
11:00-13:00	**Electrical, Electronic and Electromechanical (EEE) Parts in the New Space Paradigm: *When is Better the Enemy of Good Enough?*** K. A. LaBel (NASA, USA) **Space and Earth Radiation Environments.** M. Famá (ARSAT, Argentina)	**On-Board-Computer of a Nanosat Built With COTS Circuits** A. Parra (BBS, Argentine) **Introduction to radiation induced nanoelectronic transport degradation.** I.S. Esqueda (University of Southern California, USA)	**Development of a Hardened 150nm Standard Cell Library** JB. Dos Santos (SMDH / UFSM, Brazil) **Hardening-by-Design Techniques for Analog and Mixed-Signals** D. Loveless (University of Tennessee, USA)	**SEE Effects in FPGA: Modeling and Experimental Characterization** C. Thibeault (ETS, Canada) **Mitigating SEU and MBU Using Backward Error Recovery Approach in SRAM Based FPGA** F. Ghaffari (ETIS, France)
13:00 – 14:00	Lunch	Lunch	Lunch	Lunch
14:00 – 16:30	**Single Event Effects Test Methods** K. Tapero (RISI, Russia) **Accurate Abstraction and High Level Modeling and Validation of SEE in Electronic Systems,** O. Ait Mohamed (Concordia Univ., Canada) and Y. Savaria (Polytechnique Montréal, Canada).	**Fault Injection Methodologies** L. Entrena (UCIII, Spain) **Fault Injection Methodologies - Practical Aspects** M-A. Aguirre (University of Sevilla, Spain) **Laser Testing Laser Simulation Test Possibilities and Facilities** D. McMorrow (NRL, USA) and P. Fouillat (IMS, France)	Industrial visit + Gala Diner	**Microprocessor Testing: Characterization Tests, Mitigation** H. Quinn (LANL, USA) **RADARSAT II PowerPC 603e Processor; SEU Mitigation and on Orbit Results** H. Rufenacht, P. Allan and C. Decoust (MDA, Canada)
16:30-17:00	Break & Poster Session	Break & Poster Session		Break & Poster Session
17:00-18:00	End of the First Day	**SEE Effects on VLSI Devices (ASIC and FPGA)** L. Sterpone (POLITO, Italy)		**Error-Rate Prediction For Programmable Circuits: Methodology, Tools and Studied Cases & Concluding Remarks** R. Velazco (TIMA, France) P. Fouillat (IMS, France)